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| PHILPOTT, JUSTIN M | |

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DATE MAILED: 11/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/081,055 | KARUPPIAH, ETTIKAN K. | |
| | Examiner | Art Unit | |
| | Justin M. Philpott | 2616 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *16 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Arguments*

1. Applicant's arguments, see pages 9-10, filed August 16, 2006, with respect to the objection of the specification and the objection of claim 9 have been fully considered and are persuasive. The objection of the specification and of claim 9 has been withdrawn.

Specifically, with respect to applicant's statement that "Intel Corporation has taken the position that they prefer to omit summaries in their applications" in response to Examiner's objection of the specification for failing to include a "summary of the invention" section, it is noted herein that applicant has chosen not to follow the guidelines of 37 CFR 1.73 which states, "[a] brief summary of the invention indicating its nature and substance, which may include a statement of the object of the invention, *should* precede the detailed description" (emphasis added). Because this section recites "should" as opposed to "must" or other similar language, however, the objection of the specification is withdrawn.

2. Applicant's arguments filed August 16, 2006 have been fully considered but they are not persuasive.

Regarding claims 1 and 5, applicant argues (pages 10-13) that Cheriton does not teach a routing address "builds" a virtual path cache entry but, rather, only "checks" whether such an entry exists. However, as discussed in the previous office action, and repeated herein, Cherton provides such a claimed teaching at, e.g., col. 11, lines 41-42; virtual path cache 415 in FIG. 4 and col. 8, line 23 – col. 9, line 60. Specifically, FIG. 4 clearly identifies a "virtual path cache

415". While Cheriton may not specifically disclose the words "building" or "built" in the described invention, the "virtual path cache 415" of Cheriton is inherently "built" as broadly recited in applicant's claims. Applicant's argument to the contrary is not persuasive.

Regarding claim 12, applicant argues (pages 13-14) that Cheriton does not teach determining route identification operations based upon one or more non-zero values in the address comparison result. However, as discussed in the previous office action, and repeated herein, while Cheriton may not specifically disclose the one or more values are specifically non-zero, the values in Cheriton comprise a 15-bit index (e.g., see col. 9, lines 48-60) wherein all but one out of $2^{15}$ (i.e., 1 out of 32,768) possible index values would comprise at least one or more non-zero values. That is, in Cheriton, it is only possible for one index (i.e., 000000000000000) out of a possible 32,768 to not comprise at least one or more non-zero value. Furthermore, an index comprised entirely of zeroes is well known in the art to frequently be reserved for a null or error output. Thus, at the time of the invention it would have been obvious to one of ordinary skill in the art to implement the system of Cheriton with index values comprising at least one non-zero since it is only possible for one index (i.e., 000000000000000) out of a possible 32,768 to not comprise at least one or more non-zero values, and since an index comprised entirely of zeroes is well known in the art to be reserved for a null or error output. Accordingly, applicant's argument that claim 12 should be allowed is not persuasive in view of the teachings of Cheriton.

Regarding claim 17, applicant argues (pages 14-16) that Cheriton does not teach determining a set of route identification operations to be performed. However, as discussed in the previous office action, and repeated herein, Cheriton teaches determining a set of route

identification operations to perform (e.g., determining which virtual path record to output, see col. 9, lines 34-43). Thus, applicant's argument is not persuasive.

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-4, 7-9, 17-19, 24 and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,091,725 to Cheriton et al.

Regarding claim 1, Cheriton teaches a machine-implemented method comprising: receiving a routing address (e.g., source address 702 or destination address 701, see FIG. 7) comprising at least two routing identifiers (e.g., see the at least two paths between addresses 701/702 to 703 comprising low-order bits of source and destination addresses, respectively, see also col. 9, lines 52-60); and building a routing matrix (e.g., table of routing information, see col. 11, lines 41-42, and also see virtual path cache 415 in FIG. 4 and col. 8, line 23 – col. 9, line 60) to use in determining route identification operations to be performed (e.g., determining virtual path record to output, see col. 9, lines 34-43), the routing matrix (e.g., at virtual path cache 415) identifying one or more of the at least two routing identifiers that are to be used in routing (e.g., see col. 8, line 23 – col. 9, line 60 whereby the low-order 15 bits of each source/destination address are identified).

Regarding claim 2, Cheriton teaches the routing address comprises a destination address (e.g., destination address 701), and wherein building the routing matrix (e.g., virtual path cache 415) comprises comparing the destination address (e.g., destination address 701) with a source address (e.g., source address 702) to identify a difference (e.g., via Exclusive-OR 703, see col. 9, lines 29-60).

Regarding claim 3, Cheriton teaches comparing the destination address comprises: performing an EXCLUSIVE OR operation (e.g., via Exclusive-OR 703, see col. 9, lines 29-60) of the destination address (e.g., destination address 701) and the source address (e.g., source address 702) to produce an address comparison result (e.g., cache index 632, see col. 9, lines 29-60).

Regarding claim 4, Cheriton teaches comparing the destination address (e.g., destination address 701) comprises using parallel processing to compare the destination address (e.g., destination address 701) with the source address (e.g., source address 702) (e.g., see col. 9, lines 34-60 and FIG. 6 regarding parallel processing via parallel sets of SRAMS 601-604).

Regarding claim 7, Cheriton teaches building the routing matrix (e.g., comprising virtual path cache 415) comprises using parallel processing to build the routing matrix (e.g., see col. 9, lines 34-60 and FIG. 6 regarding parallel processing via parallel sets of SRAMS 601-604).

Regarding claim 8, Cheriton teaches determining a set of route identification operations to perform based on the routing matrix (e.g., comprising virtual path cache 415) (e.g., determining which virtual path record to output, see col. 9, lines 34-43).

Regarding claim 9, Cheriton teaches the routing matrix (e.g., comprising virtual path cache 415) consists of a binary number (see col. 9, lines 22-60 regarding low-order 15 bits, inherently a binary number).

Regarding claim 17, Cheriton teaches a system comprising: a processor (e.g., CPU 411 in combination with switch hardware 409, see FIG. 4, inherently within the network switching devices 101-104/400, see col. 8, lines 24-31); a network device (e.g., one of client computers 121-125, see FIG. 1); a first bus (e.g., one of links 110-115) coupled with the network device (e.g., one of 121-125) and with the processor (e.g., CPU 411, via coupled elements between CPU 411 and inputs/outputs 401-408); a memory system (e.g., comprising virtual path cache 415 in combination with buffer memory 410, see FIGS. 4 and 6, and col. 9, lines 21-23) embodying information indicative of instructions (e.g., see col. 8, lines 43-52 regarding instructions in buffer memory 410) to cause the processor (e.g., CPU 411 in combination with switch hardware 409) to perform operations (e.g., see col. 8, lines 43-52) comprising receiving a source address (e.g., source address 702, see FIG. 7) and a destination address (e.g., destination address 701) (e.g., see col. 8, line 24 – col. 9, line 60), each comprising at least two routing identifiers (e.g., see the at least two paths between addresses 701/702 to 703 comprising low-order bits of source and destination addresses, respectively, see also col. 9, lines 52-60), and determining a set of route identification operations to perform (e.g., determining which virtual path record to output, see col. 9, lines 34-43) based upon one or more differences between the source address routing identifiers and the destination address routing identifiers (e.g., see FIGS. 4 and 6, wherein path record at 633 is based upon cache index 632); and a second bus (e.g., virtual path record bus 633,

see FIG. 4) coupled with the memory system (e.g., at the virtual path cache 415) and with the processor (e.g., at the switch hardware 409).

Regarding claim 18, Cheriton teaches the processor (e.g., CPU 411 in combination with switch hardware 409) comprises a parallel, hardware-based multithreaded processor (e.g., see col. 9, line 61 – col. 11, line 5 and FIGS. 4 and 8).

Regarding claim 19, Cheriton teaches the network device comprises a media access controller device (e.g., see col. 5, lines 8-13 regarding the invention utilizing media access control).

Regarding claim 24, Cheriton teaches a communication system comprising: a processor (e.g., CPU 411 in combination with switch hardware 409, see FIG. 4, inherently within the network switching devices 101-104/400, see col. 8, lines 24-31); means for receiving a source address (e.g., source address 702, see FIG. 7) and a destination address (e.g., destination address 701) (e.g., see col. 8, line 24 – col. 9, line 60), each comprising at least two routing identifiers (e.g., see the at least two paths between addresses 701/702 to 703 comprising low-order bits of source and destination addresses, respectively, see also col. 9, lines 52-60); means for using the processor to identify one or more differences between the source address routing identifiers and the destination address routing identifiers (e.g., via Exclusive-OR 703, see col. 9, lines 52-60); means for identifying a set of route identification operations based upon the one or more differences (e.g., determining which virtual path record to output, see col. 9, lines 34-43), wherein a different route identification operation is determined for each of the one or more differences and see FIGS. 4 and 6, wherein path record at 633 is based upon cache index 632);

and for routing data based upon the set of route identification operations (e.g., see col. 9, line 61 – col. 11, line 5).

Regarding claim 25, Cheriton teaches the processor (e.g., CPU 411 in combination with switch hardware 409) comprises a parallel, hardware-based multithreaded processor (e.g., see col. 9, line 61 – col. 11, line 5 and FIGS. 4 and 8).

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 5, 6, 12-16 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheriton et al.

Regarding claims 5 and 6, Cheriton teaches the method discussed above regarding claim 4, however, may not specifically disclose comparing the destination address using blocks comprising four-bit blocks and/or blocks smaller than a length of the two or more routing identifiers. However, it is generally considered to be within the ordinary skill in the art to adjust, vary, select or optimize the numerical parameters or values of any system absent a showing of criticality in a particular recited value. The burden of showing criticality is on Appellant. In re Mason, 87 F.2d 370, 32 USPQ 242 (CCPA 1937); Marconi Wireless Telegraph Co. v. U.S., 320 U.S. 1, 57 USPQ 471 (1943); In re Schneider, 148 F.2d 108, 65 USPQ 129 (CCPA 1945); In re Aller, 220 F.2d 454, 105 USPQ 233 (CCPA 1955); In re Saether, 492 F.2d 849, 181 USPQ 36

(CCPA 1974); In re Antonie, 559 F.2d 618, 195 USPQ 6 (CCPA 1977); In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). Furthermore, Cherion specifically discloses that the cache may comprise various sizes (e.g., see col. 9, lines 24-28). Thus, at the time of the invention it would have been obvious to one of ordinary skill in the art to compare the destination address using blocks of a certain size, such as smaller than a length of a shortest of the two or more routing identifiers or blocks comprising four-bit blocks, since it is generally considered to be within the ordinary skill in the art to adjust, vary, select or optimize the numerical parameters or values of any system absent a showing of criticality in a particular recited value and since Cherion specifically discloses that the cache may comprise various sizes (e.g., see col. 9, lines 24-28).

Regarding claim 12, Cheriton teaches a machine-readable medium embodying information indicative of instructions for causing a machine to perform operations comprising: receiving a source address (e.g., source address 702, see FIG. 7) and a destination address (e.g., destination address 701), each comprising at least two routing identifiers (e.g., see the at least two paths between addresses 701/702 to 703 comprising low-order bits of source and destination addresses, respectively, see also col. 9, lines 52-60); performing an EXCLUSIVE OR operation of the source address routing identifiers with the destination address routing identifiers (e.g., via Exclusive-OR 703, see col. 9, lines 52-60) to produce an address comparison result (e.g., cache index 632); determining a set of route identification operations to perform (e.g., determining which virtual path record to output, see col. 9, lines 34-43) based upon one or more values in the address comparison result (e.g., see FIGS. 4 and 6, wherein path record at 633 is based upon

cache index 632), wherein a different route identification operation (e.g., which virtual path record to output, see col. 9, lines 34-43) is to be used for each of the one or more values.

Further, while Cheriton may not specifically disclose the one or more values are specifically non-zero, the values in Cheriton comprise a 15-bit index (e.g., see col. 9, lines 48-60) wherein all but one out of $2^{15}$ (i.e., 1 out of 32,768) possible index values would comprise at least one or more non-zero values. That is, in Cheriton, it is only possible for one index (i.e., 000000000000000) out of a possible 32,768 to not comprise at least one or more non-zero value. Furthermore, an index comprised entirely of zeroes is well known in the art to frequently be reserved for a null or error output. Thus, at the time of the invention it would have been obvious to one of ordinary skill in the art to implement the system of Cheriton with index values comprising at least one non-zero since it is only possible for one index (i.e., 000000000000000) out of a possible 32,768 to not comprise at least one or more non-zero values, and since an index comprised entirely of zeroes is well known in the art to be reserved for a null or error output.

Regarding claim 13, Cheriton teaches route identification operations include a direct lookup operation (e.g., see col. 8, lines 32-42).

Regarding claims 14 and 15, Cheriton teaches the method discussed above regarding claim 13, however, may not specifically disclose comparing the destination address using blocks comprising four-bit blocks and/or blocks smaller than a length of the two or more routing identifiers. However, it is generally considered to be within the ordinary skill in the art to adjust, vary, select or optimize the numerical parameters or values of any system absent a showing of criticality in a particular recited value. The burden of showing criticality is on Appellant. In re Mason, 87 F.2d 370, 32 USPQ 242 (CCPA 1937); Marconi Wireless Telegraph Co. v. U.S., 320

U.S. 1, 57 USPQ 471 (1943); In re Schneider, 148 F.2d 108, 65 USPQ 129 (CCPA 1945); In re Aller, 220 F.2d 454, 105 USPQ 233 (CCPA 1955); In re Saether, 492 F.2d 849, 181 USPQ 36 (CCPA 1974); In re Antonie, 559 F.2d 618, 195 USPQ 6 (CCPA 1977); In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). Furthermore, Cherion specifically discloses that the cache may comprise various sizes (e.g., see col. 9, lines 24-28). Thus, at the time of the invention it would have been obvious to one of ordinary skill in the art to compare the destination address using blocks of a certain size, such as smaller than a length of a shortest of the two or more routing identifiers or blocks comprising four-bit blocks, since it is generally considered to be within the ordinary skill in the art to adjust, vary, select or optimize the numerical parameters or values of any system absent a showing of criticality in a particular recited value and since Cherion specifically discloses that the cache may comprise various sizes (e.g., see col. 9, lines 24-28).

Regarding claim 16, Cheriton teaches the method discussed above regarding claim 15, however, may not specifically disclose the routing identifiers conform to an addressing architecture defined by Internet Engineering Task Force (IETF). However, Cherion clearly teaches a routing method as discussed above regarding claim 15, and IETF defines standards well known in the art for routing methods. Furthermore, it is well known in the art that applying a well known standard, or protocol, to a system provides the system with significantly improved industrial applicability. Thus, at the time of the invention it would have been obvious to one of ordinary skill in the art to apply the IETF addressing architecture standard to the system of Cherion in view of AAPA , since it is well known in the art that applying a well known standard, or protocol, to a system provides the system with significantly improved industrial applicability.

Regarding claim 20, Cheriton teaches the system discussed above regarding claim 19, however, may not specifically disclose the first bus comprises a 128-bit FIFO bus. However, Examiner takes official notice that it is well known in the art for a bus such as that in Cheriton advantageously comprises a FIFO bus in order to provide fair processing by processing packets in the order they are received on the bus. Furthermore, while a FIFO that is 128-bits wide is not specifically disclosed by Cheriton, it is generally considered to be within the ordinary skill in the art to adjust, vary, select or optimize the numerical parameters or values of any system absent a showing of criticality in a particular recited value. The burden of showing criticality is on Appellant. In re Mason, 87 F.2d 370, 32 USPQ 242 (CCPA 1937); Marconi Wireless Telegraph Co. v. U.S., 320 U.S. 1, 57 USPQ 471 (1943); In re Schneider, 148 F.2d 108, 65 USPQ 129 (CCPA 1945); In re Aller, 220 F.2d 454, 105 USPQ 233 (CCPA 1955); In re Saether, 492 F.2d 849, 181 USPQ 36 (CCPA 1974); In re Antonie, 559 F.2d 618, 195 USPQ 6 (CCPA 1977); In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). Thus, at the time of the invention it would have been obvious to one of ordinary skill in the art to provide the first bus of Cheriton with a 128-bit wide FIFO bus, since it is generally considered to be within the ordinary skill in the art to adjust, vary, select or optimize the numerical parameters or values of any system absent a showing of criticality in a particular recited value.

7. Claims 10, 11 and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheriton in view of applicant's admitted prior art (AAPA).

Regarding claims 10 and 21, Cheriton teaches the method and system discussed above regarding claims 8 and 18, respectively, and further, teaches route identification operations

include a direct lookup operation (e.g., see col. 8, lines 32-42) and a hash table lookup operation (e.g., see col. 9, lines 22-60). While Cheriton may not specifically disclose route identification operations further include a longest-prefix match lookup operation, Applicant admits that it is well known in the art for route identification operations to include a longest-prefix match lookup operation (e.g., see applicant's specification, page 3, paragraph 0007 regarding "[i]n traditional CIDR ... a longest-match-is-best approach is used"). Thus, at the time of the invention it would have been obvious to one of ordinary skill in the art to implement the route identification operations routing method of Cheriton to further include a longest-prefix match lookup operation, since Applicant admits that it is well known in the art for route identification operations to include a longest-prefix match lookup operation, and it would have been obvious to one of ordinary skill in the art to utilize such a well known routing teaching in the art in the routing method of Cheriton in order to provide enhanced operation and industrial applicability.

Regarding claim 11, Cheriton in view of AAPA teach the method discussed above regarding claim 10, however, may not specifically disclose the routing identifiers conform to an addressing architecture defined by Internet Engineering Task Force (IETF). However, Cherion in view of AAPA clearly teaches a routing method as discussed above regarding claim 10, and IETF defines standards well known in the art for routing methods. Furthermore, it is well known in the art that applying a well known standard, or protocol, to a system provides the system with significantly improved industrial applicability. Thus, at the time of the invention it would have been obvious to one of ordinary skill in the art to apply the IETF addressing architecture standard to the system of Cherion in view of AAPA , since it is well known in the art that applying a well

known standard, or protocol, to a system provides the system with significantly improved industrial applicability.

Regarding claim 22, Cheriton teaches the memory system (e.g., comprising virtual path cache 415 in combination with buffer memory 410, see FIGS. 4 and 6, and col. 9, lines 21-23) comprises a dynamic random access memory (e.g., shared buffer memory 410, see col. 8, lines 24-61) and a static random access memory (e.g., SRAM 601-604 in virtual cache 415).

Regarding claim 23, Cheriton teaches the second bus (e.g., virtual path record bus 633) comprises a peripheral component interconnect bus (e.g., coupling to ports 401-408 via switch 409, see FIG. 4).

***Conclusion***

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin M. Philpott whose telephone number is 571.272.3162. The examiner can normally be reached on M-F, 9:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on 571.272.3179. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Justin M. Philpott

CHI PHAM
SUPERVISORY PATENT EXAMINER 10/30/06